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Efficient BIST architecture to detect defects in TSVs

A new BIST (Built-in Self-Test) architecture has been developed to detect defects in TSVs (Through Silicon Vias) during the pre-bond phase. A simple circuit is included to detect defective TSVs affected by hard and/or weak defects, adding low area overhead and applying a simple and fast test methodology. The same circuit can be subsequently re-used for reconfiguration if a defective TSV has been detected. Partners to further develop the technology and/or to establish commercial agreements along with technical cooperation are sought.

The Challenge

Three-dimensional integrated circuits (3-D ICs) have arisen as a promising solution to attend the continuously increasing demands from the semiconductor industry. A 3-D IC integrates in a single package a vertical stack of tiers interconnected by means of Through Silicon Vias (TSVs). TSVs are critical elements susceptible to undergo defects during the manufacturing process. The detection of defective TSVs in the earliest process step is a key factor to prevent yield loss. Hence, specific testing of TSVs are done before every tier is stack, the so-called pre-bond test. However, pre-bond testing is still challenging. TSVs are too small for pre-bond test probe and present built-in self test (BIST) architectures suffer from some disadvantages, namely: lack for detection for weak defects, large area overhead and long test application times. In this context, new test approaches are required to efficiency detect defects in TSVs during the pre-bond test.

The Technology

The present invention allows to perform a fast and effective test of TSVs structures during the pre-bond phase by comparing the behavior between the TSV under test and a reference element. The invention takes into account that TSVs has only a terminal accessible during this stage of the manufacturing process. The reference element is a spare TSV included commonly for reconfiguration purposes. The same spare TSV can be used to test a set of TSVs, minimizing area overhead. The BIST architecture is a small and simple circuit so that it can subsequently re-used for reconfiguration purposes if a defective TSV is detected.

Innovative advantages

- Detection of common hard and weak defects affecting TSVs.
- Fast and simple test methodology.
- Low area overhead.
- Re-use of the architecture for subsequent reconfiguration, if required.

Current stage of development

Successful electrical simulations results have been obtained for different technology nodes, including process variations.

Applications and Target Market

The technology can be of especial interest to semiconductors manufacturers of 3-D ICs.

Reference number

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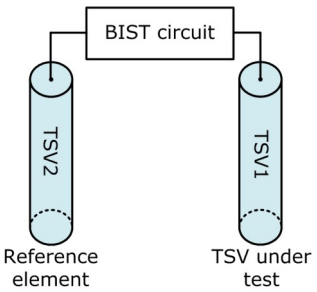
A Built-in Self-Test architecture to detect hard and weak defects in TSVs during the pre-bond phase



Behavior comparison between the TSV under test and a reference element

A simple circuit with low area overhead and re-use for reconfiguration purposes.

Business Opportunity

Technology available for licensing with technical cooperation

Patent Status

Priority application

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